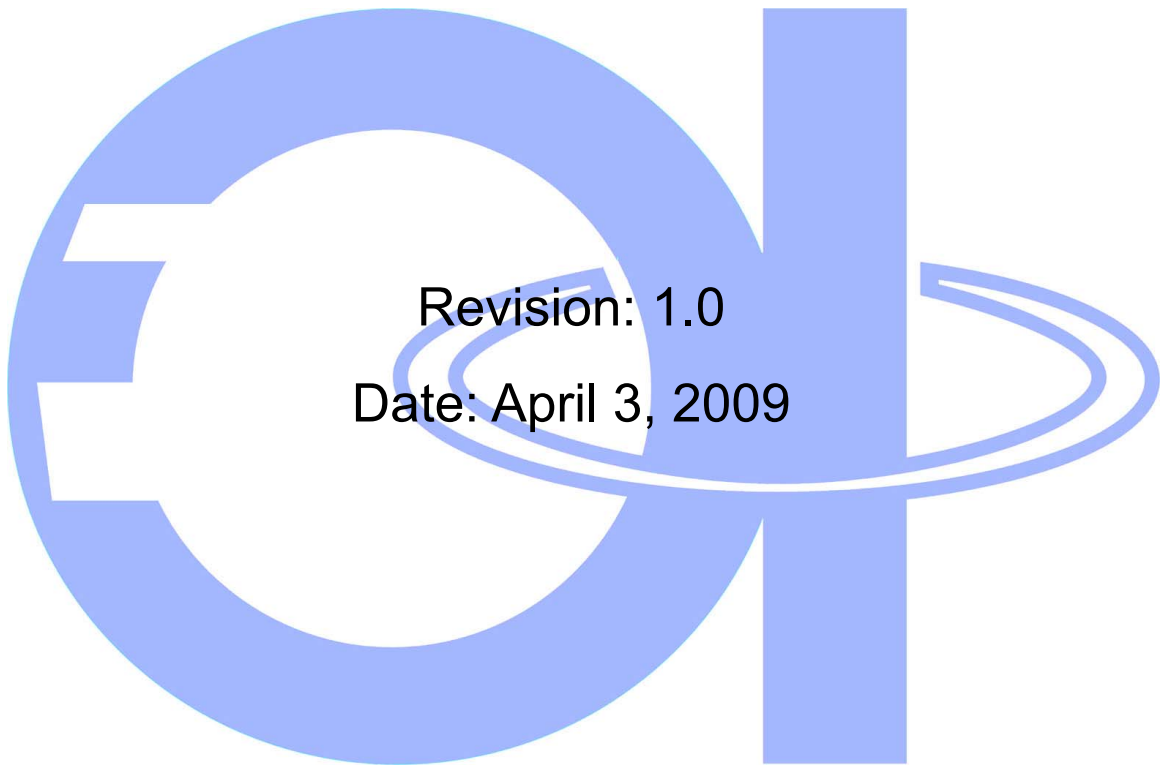


# **JL4229A**

## ***Multimedia Controller***



Revision: 1.0

Date: April 3, 2009

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0. Revision History

Revision	Description of Changes	Date
1.0	Initial Release	2009/4/3



## 1. General Description

JL4229A is a highly integrated multimedia controller targeted for Digital Photo Frame with [digital LCD panel through LVDS interface](#). It is capable of reading/playing the photo (JPEG), video (Motion JPEG), and audio (MP3/WMA) from memory cards and internal NAND Flash. All of your favorite digital photos can be played back in slide show or in still display while MP3/WMA music is playing back. There are various slide transition effect are added between each photo slide. All of above playback doesn't need the use of PC. It can read/write the files from/to different kinds of memory card such as USB Pen Drive, CF/Microdrive, SD/SDHC, MMC/MMCplus, MS/MS PRO, XD, and NAND Flash. Besides photo frame function, JL4229A can be used as USB Card Reader thru USB Device port (MassStorage).

## 2. Features

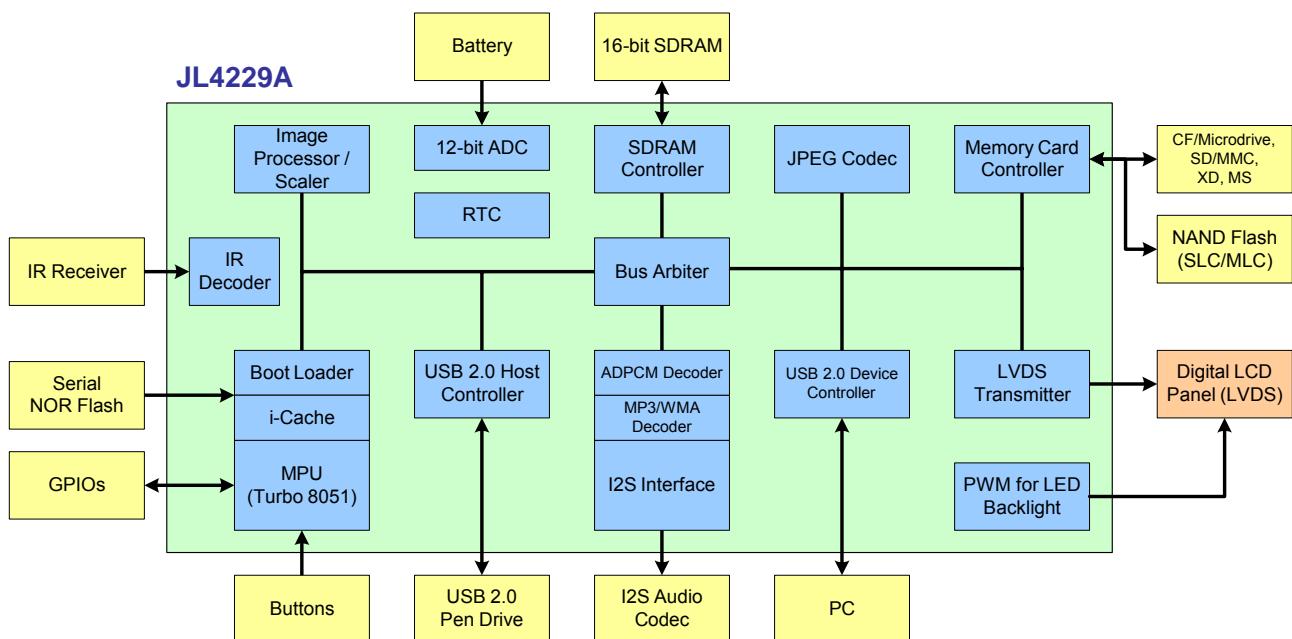
- Embedded 8-bit 8051 MCU
  - Firmware is booted up from either Serial NOR Flash or SLC NAND Flash memory.
  - Support in-system programming (ISP) Function
- Program Boot-up Source
  - Serial NOR Flash
  - SLC NAND Flash
- Display
  - Integrated TCON
  - Support Digital (LVDS) LCD Panel
  - Embedded LVDS Transmitter to convert 28-bit data into 4-pair LVDS data stream
  - Built-in one PWM for LED backlight control, or charge pump circuit
- OSD
  - Font-based OSD
  - Graphic-based OSD
  - Supported Language : English, 正體中文, 簡體中文, 日本語, Deutsch, Français, Español, Italiano, Nederlands, Русская, Português, Dansk, Ελληνικά, Norsk, Svenska, Suomi
- Photo Playback
  - JPEG
    - ✓ Support baseline and progressive JPEG
    - ✓ Support photo resolution up to 16,384 x 16,384 pixels
    - ✓ High-speed JPEG compression/decompression rate: 27 mega pixels per second
  - BMP
    - ✓ Support Windows V3 and OS/2 V1 header
    - ✓ Color Depth : 24 bits per pixel
- Video Playback



- Support Motion JPEG only
- Audio format : PCM Format 、ADPCM Format
- Video resolution and frame rate : QVGA@60fps, VGA@30fps
- Audio Playback
  - MP3 / WMA
  - Support MP3 Lyrics and ID3 Tag
  - 8/16-bit PCM, 4-bit IMA-ADPCM audio codec
  - I<sup>2</sup>S interface for external audio DAC to drive earphone or speaker
- Storage Interface
  - CompactFlash Interface
    - ✓ Comply with CF+ and CompactFlash Specification Revision 3.0
  - IDE Interface
    - ✓ Comply with ATA /ATAPI-6 Specification Rev 2.0
    - ✓ Support PIO mode 0~4, Multiword DMA mode 0~2, and Ultra DMA mode 0~5
  - SD/MMC Interface
    - ✓ Comply with SD 2.0 (backward compatible to SD 1.1)
    - ✓ Comply with MMC 4.0 (backward compatible to MMC 3.x)
  - Memory Stick/Memory Stick PRO Interface
    - ✓ Comply with MS v1.40
    - ✓ Comply with MS PRO v1.03
  - SmartMedia and xD Interface
    - ✓ Comply with SmartMedia v1.0
    - ✓ Comply with xD-Picture Card v1.2
  - SLC/MLC NAND Flash Memory
    - ✓ Support 1-bit ECC per 256 bytes (Hamming Codec)
    - ✓ Support 4-bit ECC per 512 bytes (RS Codec)
- USB Interface
  - Support Mass-Storage Class for both Device and Host interface
  - USB 2.0 Device
    - ✓ High Speed and Full Speed USB 2.0 Device with embedded USB PHY
  - USB 2.0 Host
    - ✓ High Speed and Full Speed USB 2.0 Host with embedded USB PHY
- Image Display Functions
  - Preview, Slideshow, Zoom In / Out, Pan, Rotate, and so on
  - Image Rotation: 90 degrees in clockwise or counter-clockwise direction
  - Excellent image scaling engine
  - Picture-In-Picture display

- 2D Edge Enhancement (Image Sharpness)
- Gamma Correction, Brightness / Contrast Adjustment
- SDRAM interface
  - Support 16-bit SDRAM up to 16Mx16 bits
- Provide UART, SPI-master and I<sup>2</sup>C-master serial interfaces
- Integrated RTC
- Integrated IR Decoder
  - Support NEC Transmission Format
- Embedded 12-bit ADC for low battery detection or other application
- Package : 216-pin LQFP (24x24mm)

### 3. Block Diagram



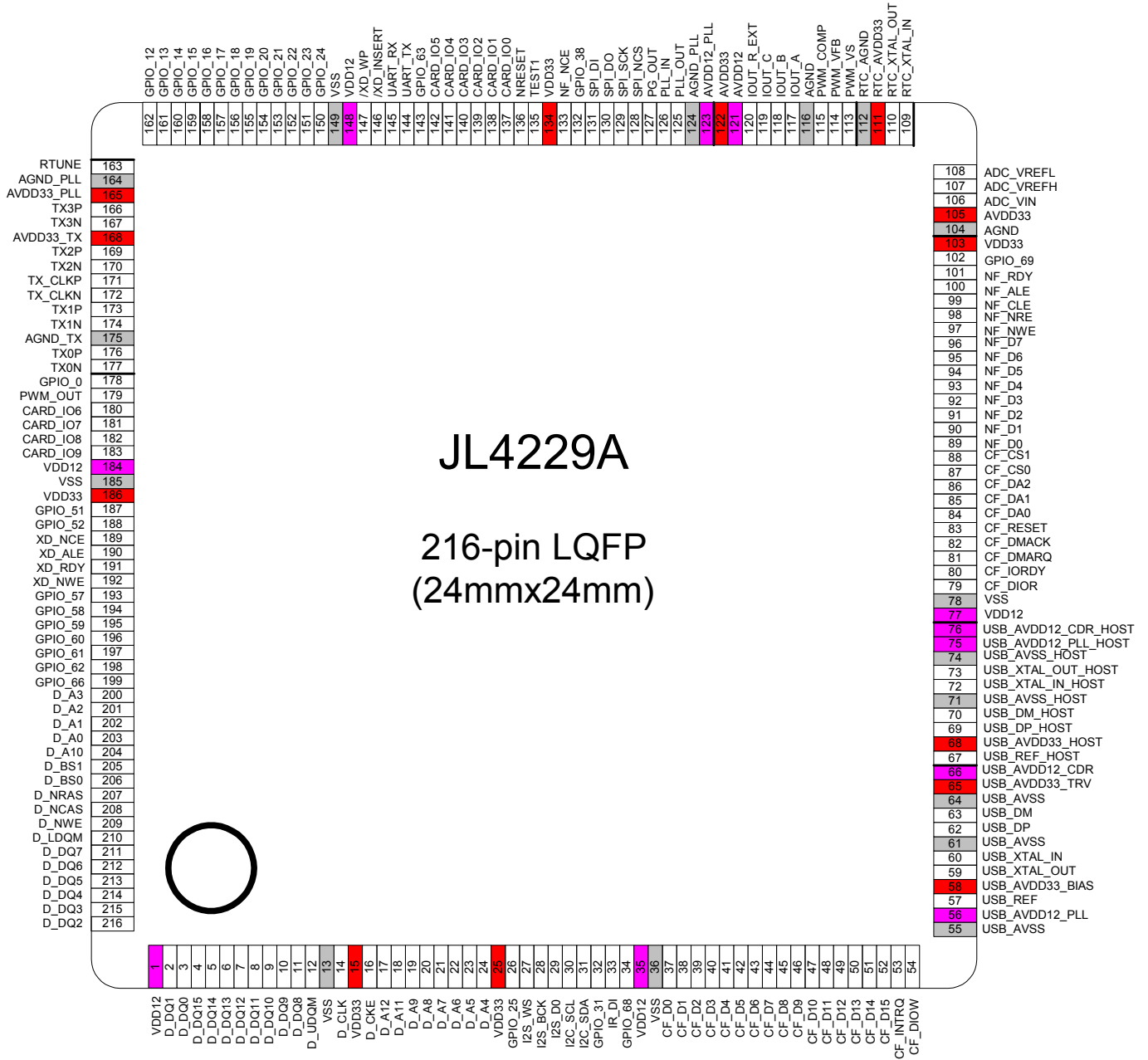
### 4. Applications

- Digital Photo Frame (DPF)
  - Viewing Photos (JPEG)
  - Viewing Movie (Motion JPEG AVI)
  - Listening to MP3/WMA music
- USB2.0 Card Reader
- DPF with Clock/Calendar/Alarm



### 5. Pin Assignment and Pin Description

#### 5.1 Pin Assignment





## 5.2 Pin Description

Pin #	Pin name	Type	Description	Memo
1	VDD12	P	Core power 1.2V	
2	D_DQ1	B8	SDRAM data bus 1	
3	D_DQ0	B8	SDRAM data bus 0	
4	D_DQ15	B8	SDRAM data bus 15	
5	D_DQ14	B8	SDRAM data bus 14	
6	D_DQ13	B8	SDRAM data bus 13	
7	D_DQ12	B8	SDRAM data bus 12	
8	D_DQ11	B8	SDRAM data bus 11	
9	D_DQ10	B8	SDRAM data bus 10	
10	D_DQ9	B8	SDRAM data bus 9	
11	D_DQ8	B8	SDRAM data bus 8	
12	D_UDQM	O8	SDRAM high byte data write mask, it must be connected to pull-down 8.2 K ohm resistor	
13	VSS	G	Ground	
14	D_CLK	O16	SDRAM clock	
15	VDD33	P	I/O power 3.3V	
16	D_CKE	O8	SDRAM clock enable	
17	D_A12	O8	SDRAM address bus 12	
18	D_A11	O8	SDRAM address bus 11	
19	D_A9	O8	SDRAM address bus 9	
20	D_A8	O8	SDRAM address bus 8	
21	D_A7	O8	SDRAM address bus 7	
22	D_A6	O8	SDRAM address bus 6	
23	D_A5	O8	SDRAM address bus 5	
24	D_A4	O8	SDRAM address bus 4	
25	VDD33	P	I/O power 3.3V	
26	GPIO_25	B2	General purpose IO #25	
27	I2S_WS	O2	I <sup>2</sup> S word select output	GPIO_26
28	I2S_BCK	O2	I <sup>2</sup> S serial clock output	GPIO_27
29	I2S_DO	O2	I <sup>2</sup> S serial data output	GPIO_28
30	I2C_SCL	OD	I <sup>2</sup> C serial clock output	GPIO_29
31	I2C_SDA	BD	I <sup>2</sup> C serial data	GPIO_30
32	GPIO_31	B2	General purpose IO #31	
33	IR_DI	I	Data input of remote control	GPIO_32



Pin #	Pin name	Type	Description	Memo
34	GPIO_68	B2	General purpose IO #68	
35	VDD12	P	Core power 1.2V	
36	VSS	G	Ground	
37	CF_D0	B4	CF data bus 0	
38	CF_D1	B4	CF data bus 1	
39	CF_D2	B4	CF data bus 2	
40	CF_D3	B4	CF data bus 3	
41	CF_D4	B4	CF data bus 4	
42	CF_D5	B4	CF data bus 5	
43	CF_D6	B4	CF data bus 6	
44	CF_D7	B4	CF data bus 7	
45	CF_D8	B4	CF data bus 8	
46	CF_D9	B4	CF data bus 9	
47	CF_D10	B4	CF data bus 10	
48	CF_D11	B4	CF data bus 11	
49	CF_D12	B4	CF data bus 12	
50	CF_D13	B4	CF data bus 13	
51	CF_D14	B4	CF data bus 14	
52	CF_D15	B4	CF data bus 15	
53	CF_INTRQ	I	CF Interrupt Request	
54	CF_DIOW	O4	CF read strobe output	
55	USB_AVSS	G	USB Device transceiver ground	
56	USB_AVDD12_PLL	P	USB Device transceiver 1.2V power for PLL	
57	USB_REF	A	Connect 12.1Kohm (1%) resistor to ground. The purpose of REF is to provide a reference for the current resource of the high-speed USB Device driver	
58	USB_AVDD33_BIAS	P	USB Device transceiver 3.3V power for BIAS	
59	USB_XTAL_OUT	A	Oscillator output. Connect to a 12Mhz crystal for USB Device transceiver	
60	USB_XTAL_IN	A	Oscillator input. Connect to a 12Mhz crystal for USB Device transceiver	
61	USB_AVSS	G	USB Device transceiver ground	
62	USB_DP	A	USB Device D+	
63	USB_DM	A	USB Device D-	
64	USB_AVSS	G	USB Device transceiver ground	
65	USB_AVDD33_TRV	P	3.3V power for USB Device transceiver	
66	USB_AVDD12_CDR	P	USB Device transceiver 1.2V power for CDR	



Pin #	Pin name	Type	Description	Memo
67	USB_REF_HOST	A	Connect 12.1Kohm (1%) resistor to ground. The purpose of REF is to provide a reference for the current resource of the high-speed USB Host driver.	
68	USB_AVDD33_HOST	P	USB Host transceiver ground	
69	USB_DP_HOST	A	USB Host D+	
70	USB_DM_HOST	A	USB Host D-	
71	USB_AVSS_HOST	G	USB Host transceiver ground	
72	USB_XTAL_IN_HOST	A	Oscillator input. Connect to a 12MHz crystal for USB Host transceiver	
73	USB_XTAL_OUT_HOST	A	Oscillator output. Connect to a 12MHz crystal for USB Host transceiver	
74	USB_AVSS_HOST	P	USB Host transceiver ground	
75	USB_AVDD12_PLL_HOST	P	USB Host transceiver 1.2V power for PLL	
76	USB_AVDD12_CDR_HOST	P	USB Host transceiver 1.2V power for CDR	
77	VDD12	P	Core Power 1.2V	
78	VSS	G	Ground	
79	CF_DIOR	O4	CF read strobe output	
80	CF_IODRY	I	CF card ready	
81	CF_DMARQ	O4	DMA acknowledge signal in true IDE mode	
82	CF_DMACK	O4	DMA request signal in true IDE mode	
83	CF_RESET	O4	CF Hardware Reset output	
84	CF_DA0	O4	CF Address Line 0	
85	CF_DA1	O4	CF Address Line 1	
86	CF_DA2	O4	CF Address Line 2	
87	CF_CS0	O4	CF Chip Select 0 in true IDE mode	
88	CF_CS1	O4	CF Chip Select 1 in true IDE mode	
89	NF_D0	B4	Data 0 of NAND Flash memory	
90	NF_D1	B4	Data 1 of NAND Flash memory	
91	NF_D2	B4	Data 2 of NAND Flash memory	
92	NF_D3	B4	Data 3 of NAND Flash memory	
93	NF_D4	B4	Data 4 of NAND Flash memory	
94	NF_D5	B4	Data 5 of NAND Flash memory	
95	NF_D6	B4	Data 6 of NAND Flash memory	
96	NF_D7	B4	Data 7 of NAND Flash memory	
97	NF_NWE	O4	Write strobe for NAND Flash memory	
98	NF_NRE	O4	Read strobe for NAND Flash memory	
99	NF_CLE	O4	Command latch enable for NAND Flash memory	



Pin #	Pin name	Type	Description	Memo
100	NF_ALE	O4	Address latch enable for NAND Flash memory	
101	NF_RDY	I	Ready signal for NAND Flash memory	GPIO_40
102	GPIO_69	B2	General purpose IO #69	
103	VDD33	P	I/O power 3.3V	
104	AGND	G	ADC ground	
105	AVDD33	P	ADC power 3.3V	
106	ADC_VIN	A	ADC analog signal input.	
107	ADC_VREFH	A	ADC reference voltage high	
108	ADC_VREFL	A	ADC reference voltage low	
109	RTC_XTAL_IN	A	Oscillator input. Connect to a 32.768 KHz crystal for RTC	
110	RTC_XTAL_OUT	A	Oscillator output. Connect to a 3.2768 KHz crystal for RTC	
111	RTC_AVDD33	P	RTC power 3.3V	
112	RTC_AGND	G	RTC ground	
113	PWM_VS	A	PWM sense voltage input	
114	PWM_VFB	A	PWM Feedback voltage input	
115	PWM_COMP	A	PWM Compensation pin	
116	AGND	G	Analog ground	
117	IOUT_A	A	Test pin	
118	IOUT_B	A	Test pin	
119	IOUT_C	A	Test pin	
120	IOUT_R_EXT	A	Test pin. This pin should be connected a resistor to ground	
121	AVDD12	P	Analog power 1.2V	
122	AVDD33	P	Analog power 3.3V	
123	AVDD12_PLL	P	PLL power 1.2V	
124	AGND_PLL	G	PLL ground	
125	PLL_OUT	O16	Test pin	
126	PLL_IN	I	Test pin	
127	PG_OUT	O2	PWM output for the external driver to control backlight brightness	GPIO_33
128	SPI_NCS	O2	SPI chip select, active low	GPIO_34
129	SPI_SCK	O2	SPI serial clock output	GPIO_35
130	SPI_DO	O2	SPI serial data output	GPIO_36
131	SPI_DI	I	SPI serial data input	GPIO_37
132	GPIO_38	B2	General purpose I/O #38	



Pin #	Pin name	Type	Description	Memo
133	NF_NCE	O4	Chip enable signal for NAND Flash	GPIO_39
134	VDD33	P	I/O power 3.3V	
135	TEST1	I	Test pin, which must be pull-high with a 10K ohms resistor	
136	NRESET	I	External reset pin, active low	Pull-up
137	CARD_IO0	O8	Memory Cards IO #0	GPIO_41
138	CARD_IO1	B4	Memory Cards IO #1	GPIO_42
139	CARD_IO2	B4	Memory Cards IO #2	GPIO_43
140	CARD_IO3	B4	Memory Cards IO #3	GPIO_44
141	CARD_IO4	B4	Memory Cards IO #4	GPIO_45
142	CARD_IO5	B4	Memory Cards IO #5	GPIO_46
143	GPIO_63	B2	General purpose I/O #63	
144	UART_TX	O2	UART transmitter output	GPIO_64
145	UART_RX	I	UART receiver input	GPIO_65
146	/XD_INSERT	I	xD Card detect signal, active low	GPIO_70
147	/XD_WP	O2	xD Card write protect, active low	GPIO_71
148	VDD12	P	Core power 1.2V	
149	VSS	G	Ground	
150	GPIO_24	B2	General purpose I/O #24	
151	GPIO_23	B2	General purpose I/O #23	
152	GPIO_22	B2	General purpose I/O #22	
153	GPIO_21	B2	General purpose I/O #21	
154	GPIO_20	B2	General purpose I/O #20	
155	GPIO_19	B2	General purpose I/O #19	
156	GPIO_18	B2	General purpose I/O #18	
157	GPIO_17	B2	General purpose I/O #17	
158	GPIO_16	B2	General purpose I/O #16	
159	GPIO_15	B2	General purpose I/O #15	
160	GPIO_14	B2	General purpose I/O #14	
161	GPIO_13	B2	General purpose I/O #13	
162	GPIO_12	B2	General purpose I/O #12	
163	RTUNE	A	Input for Bias Current Tuning (with 12KΩ to ground)	
164	AGND_PLL	G	Ground for PLL of LVDS transmitter	
165	AVDD33_PLL	P	3.3V power for PLL of LVDS transmitter	
166	TX3P	LVDS	Positive LVDS differential data output of the channel 3	



Pin #	Pin name	Type	Description	Memo
167	TX3N	LVDS	Negative LVDS differential data output of the channel 3	
168	AVDD33_TX	P	3.3V power for LVDS transmitter	
169	TX2P	LVDS	Positive LVDS differential data output of the channel 2	
170	TX2N	LVDS	Negative LVDS differential data output of the channel 2	
171	TX_CLKP	LVDS	Positive LVDS differential clock output	
172	TX_CLKN	LVDS	Negative LVDS differential clock output	
173	TX1P	LVDS	Positive LVDS differential data output of the channel 1	
174	TX1N	LVDS	Negative LVDS differential data output of the channel 1	
175	AGND_TX	G	Ground for LVDS transmitter	
176	TX0P	LVDS	Positive LVDS differential data output of the channel 0	
177	TX0N	LVDS	Negative LVDS differential data output of the channel 0	
178	GPIO_0	B4	General purpose I/O #0	
179	PWM_OUT	O24	PWM control output for external MOSFET	
180	CARD_IO6	B4	Memory Cards IO #6	GPIO_47
181	CARD_IO7	B4	Memory Cards IO #7	GPIO_48
182	CARD_IO8	B4	Memory Cards IO #8	GPIO_49
183	CARD_IO9	B4	Memory Cards IO #9	GPIO_50
184	VDD12	P	Core power 1.2V	
185	VSS	G	Ground	
186	VDD33	P	I/O power 3.3V	
187	GPIO_51	B2	General purpose I/O #51	
188	GPIO_52	B2	General purpose I/O #52	
189	XD_NCE	O2	Chip enable signal for xD Memory Card	GPIO_53
190	XD_ALE	O2	Address latch enable for xD Memory Card	GPIO_54
191	XD_RDY	I	Ready signal for xD Memory Card	GPIO_55
192	XD_NWE	O2	Write strobe for xD Memory Card	GPIO_56
193	GPIO_57	B2	General purpose I/O #57	
194	GPIO_58	B2	General purpose I/O #58	
195	GPIO_59	B2	General purpose I/O #59	
196	GPIO_60	B2	General purpose I/O #60	
197	GPIO_61	B2	General purpose I/O #61	
198	GPIO_62	B2	General purpose I/O #62	
199	GPIO_66	B2	General purpose I/O #66	



Pin #	Pin name	Type	Description	Memo
200	D_A3	O8	SDRAM address bus 3	
201	D_A2	O8	SDRAM address bus 2	
202	D_A1	O8	SDRAM address bus 1	
203	D_A0	O8	SDRAM address bus 0	
204	D_A10	O8	SDRAM address bus 10	
205	D_BS1	O8	SDRAM bank address 1	Boot Mode[1] <b>(Note 1)</b>
206	D_BS0	O8	SDRAM bank address 0	Boot Mode[0] <b>(Note 1)</b>
207	D_NRAS	O8	SDRAM row address strobe output	
208	D_NCAS	O8	SDRAM column address strobe output	
209	D_NWE	O8	SDRAM write strobe	
210	D_LDQM	O8	SDRAM low byte data write mask	Boot Mode[2] <b>(Note 1)</b>
211	D_DQ7	B8	SDRAM data bus 7	
212	D_DQ6	B8	SDRAM data bus 6	
213	D_DQ5	B8	SDRAM data bus 5	
214	D_DQ4	B8	SDRAM data bus 4	
215	D_DQ3	B8	SDRAM data bus 3	
216	D_DQ2	B8	SDRAM data bus 2	

**Note 1:**

- Pull up/down these two pins with 10K ohm resistor to select system booting method.

Boot Mode[2:0]	Function
000	Booting from the internal ROM.
001	Booting from Serial NOR Flash.
011	Booting from NAND Flash memory.
others	Reserved.

- All digital input pin can take 5V tolerance

Type	Description
P	Power pin
G	Ground pin
A	Analog pin



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I	3.3V CMOS input pin
O2	3.3V CMOS output pin with 2mA driving ability
O4	3.3V CMOS output pin with 4mA driving ability
O8	3.3V CMOS output pin with 8mA driving ability
O16	3.3V CMOS output pin with 16mA driving ability
O24	3.3V CMOS output pin with 24mA driving ability
B2	3.3V CMOS bi-direction pin with 2mA driving ability
B4	3.3V CMOS bi-direction pin with 4mA driving ability
B8	3.3V CMOS bi-direction pin with 8mA driving ability
B16	3.3V CMOS bi-direction pin with 16mA driving ability
BD	3.3V CMOS bi-direction pin with open drain output pin
OD	3.3V CMOS open drain output pin
LVDS	<a href="#">Low Voltage Differential Signaling output pin</a>



### 5.3 GPIO Mux Table

Each GPIO pin has its own function select registers, Alt[2:1], firmware can configure each GPIO pin to different function individually.

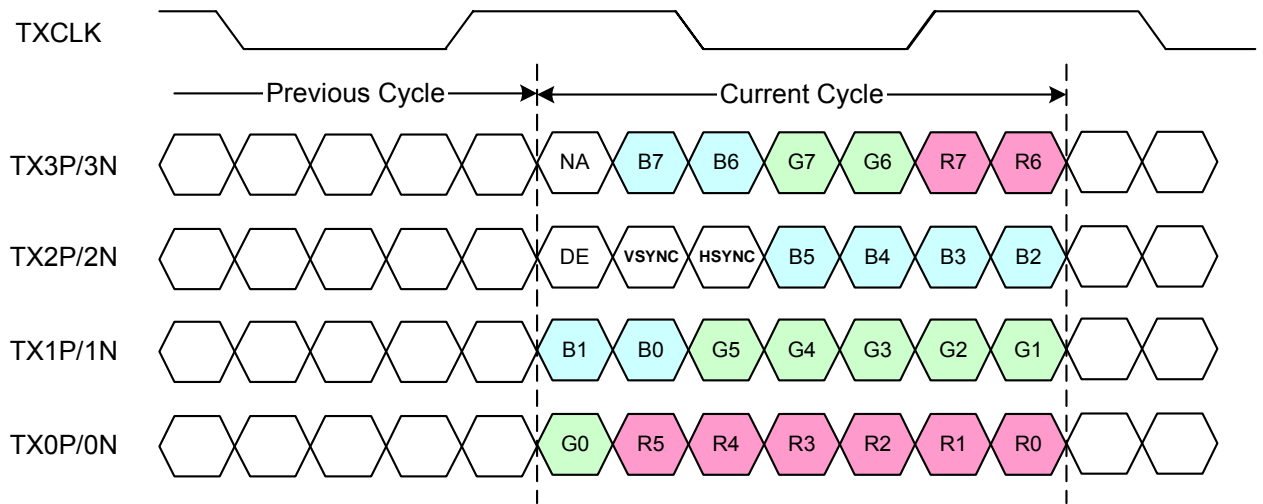
Normal Mode							
Alt[2:1]= "00"		Alt[2:1]= "01"		Alt[2:1]= "10"		Alt[2:1]= "11"	
GPIO_12	B2		O				
GPIO_13	B2		O				
GPIO_14	B2		O				
GPIO_15	B2		O				
GPIO_16	B2		O				
GPIO_17	B2		O				
GPIO_18	B2		O				
GPIO_19	B2		O				
GPIO_20	B2		O				
GPIO_21	B2		O				
GPIO_22	B2		O				
GPIO_23	B2		O				
GPIO_24	B2		O				
GPIO_25	B2			PG1_Out_0	O		
GPIO_26	B2	I2S_WS	O	RTC_CLKOUT	O		
GPIO_27	B2	I2S_BCK	O	RTC_SECOUT	O		
GPIO_28	B2	I2S_DO	O				
GPIO_29	B2	I2C_SCL	OD			UART_TX	O
GPIO_30	B2	I2C_SDA	BD			UART_RX	I
GPIO_31	B2						
GPIO_32	B2	IR_IN	I				
GPIO_33	B2	PG_OUT	O				
GPIO_34	B2	SPI_nCS	O				
GPIO_35	B2	SPI_SCK	O				
GPIO_36	B2	SPI_DO	O				
GPIO_37	B2	SPI_DI	I				
GPIO_38	B2	SPI_nCS_1	O				
GPIO_39	B16	NF_nCE1	O				
GPIO_40	B2	NF_RDY1	I				
GPIO_41	B2	SD_CLK	O	MS_SCLK	O	xD_CLE	O
GPIO_42	B2	SD_CMD	B	MS_BS	O	xD_NRE	O



Normal Mode							
Alt[2:1]= "00"		Alt[2:1]= "01"		Alt[2:1]= "10"		Alt[2:1]= "11"	
GPIO_43	B2	SD_D0	B	MS_DATA0	B	xD_D0	B
GPIO_44	B2	SD_D1	B	MS_DATA1	B	xD_D1	B
GPIO_45	B2	SD_D2	B	MS_DATA2	B	xD_D2	B
GPIO_46	B2	SD_D3	B	MS_DATA3	B	xD_D3	B
GPIO_47	B2	MMC_D4	B			xD_D4	B
GPIO_48	B2	MMC_D5	B			xD_D5	B
GPIO_49	B2	MMC_D6	B			xD_D6	B
GPIO_50	B2	MMC_D7	B			xD_D7	B
GPIO_51	B2			NF_nCE2	O		
GPIO_52	B2			NF_RDY2	I		
GPIO_53	B2	RSTS	I	NF_nCE3	O	xD_NCE	O
GPIO_54	B2	WSTS	I	NF_RDY3	I	xD_ALE	O
GPIO_55	B2	MPU_nWR	O	NF_nCE4	O	xD_RDY	I
GPIO_56	B2	MPU_nRD	O	NF_RDY4	I	xD_NWE	O
GPIO_57	B8	MS_SCLK	O			SD_CLK	O
GPIO_58	B4	MS_BS	O			SD_CMD	O
GPIO_59	B4	MS_DATA0	B			SD_D0	B
GPIO_60	B4	MS_DATA1	B			SD_D1	B
GPIO_61	B4	MS_DATA2	B			SD_D2	B
GPIO_62	B4	MS_DATA3	B			SD_D3	B
GPIO_63	B16	PG1_Out_0	O				
GPIO_64	B2	UART_TX	O				
GPIO_65	B2	UART_RX	I				
GPIO_66	B2	DDI_25	O				
GPIO_68	B2	DDI_27	O				
GPIO_69	B2						
GPIO_70	B2						
GPIO_71	B2						



### 6. LVDS Output Data Mapping





## 7. Electrical Characteristic

- Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD33/AVDD33/RTC_AVDD33/ USB_AVDD33_BIAS/AV33_PLL/ USB_AVDD33_TRV/AVDD33_TX/ USB_AVDD33_HOST	Power Supply (3.3V)	-0.3 to 3.6	V
VDD12/AVDD12/AVDD12_PLL/ USB_AVDD12_PLL/ USB_AVDD12_CDR/ USB_AVDD12_PLL_HOST/ USB_AVDD12_CDR_HOST	Power Supply (1.2V)	-0.3 to 1.32	V
ADC_VIN	Input Voltage	ADC_VREFL to ADC_VREFH	V
ADC_VREFH	Input Voltage	2.7 to AVDD33	V
ADC_VREFL	Input Voltage	0 to 0.5	V
V <sub>IN</sub>	Input Voltage	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>CC</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-55 to 150	

- Recommended Operation Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD33/AVDD33/RTC_AVDD33/ USB_AVDD33_BIAS/AV33_PLL/ USB_AVDD33_TRV/AVDD33_TX/ USB_AVDD33_HOST	Power Supply (3.3V)	3.0	3.3	3.6	V
VDD12/AVDD12/AVDD12_PLL/ USB_AVDD12_PLL/ USB_AVDD12_CDR/ USB_AVDD12_PLL_HOST/ USB_AVDD12_CDR_HOST	Power Supply (1.2V)	1.27	1.32	1.37	V
T <sub>OPR</sub>	Operating Temperature	0	25	70	



- DC Electrical Characteristics for 3.3 volts operation

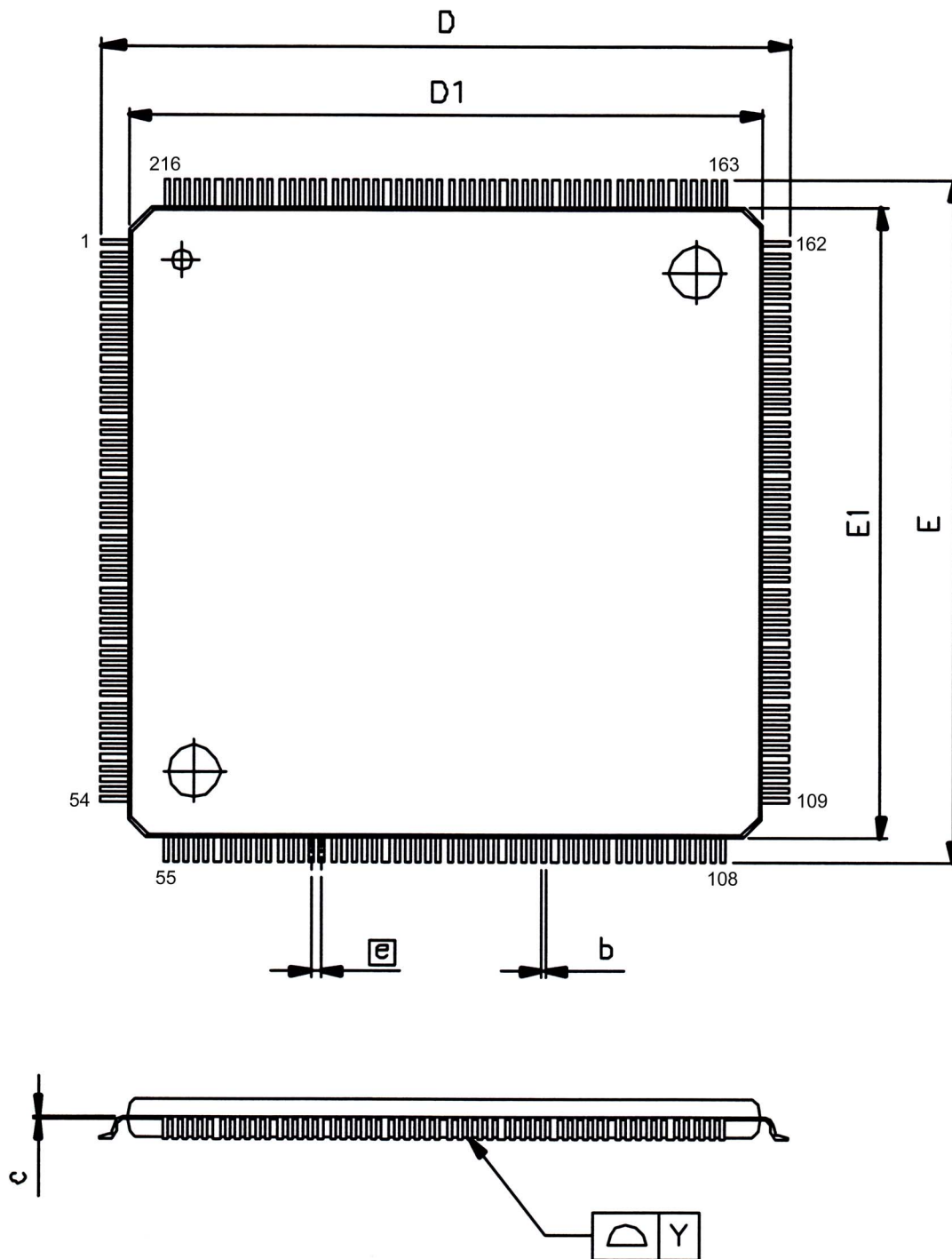
(Under Recommended Operating Conditions and  $V_{CC} = 3.0V \sim 3.6V$ ,  $T_j = 0$  to  $+70$  )

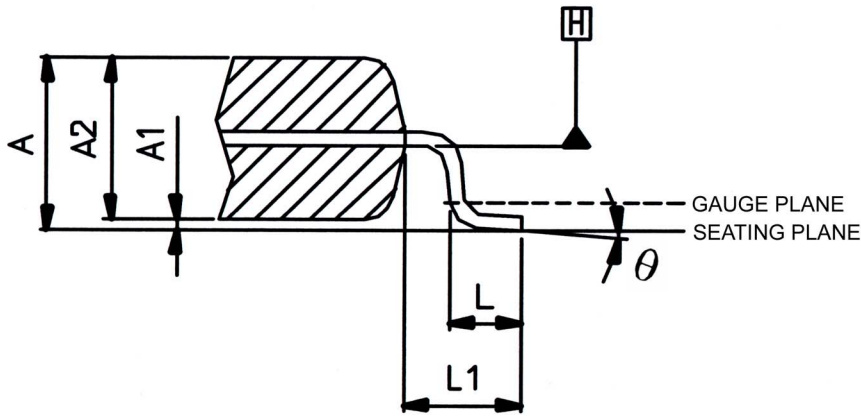
Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IL}$	Input Low Voltage	-0.3		0.8	V
$V_{IH}$	Input High Voltage	2.0		$V_{CC}+0.3$	V
$V_{T-}$	Schmitt Input Low Voltage	-0.3		0.8	V
$V_{T+}$	Schmitt Input High Voltage	2.0		$V_{CC}+0.3$	V
$V_{OL}$	Output Low Voltage			0.4	V
$V_{OH}$	Output High Voltage	2.4			V
$V_{OC(LVDS)}$	Steady-state common mode output Voltage	1.13	1.25	1.38	V
$V_{OD(LVDS)}$	Differential steady-state output Voltage (note1)	250	350	450	mV

**Note1:** Test condition at  $R_L=100\Omega$

## 8. Package Information

- Package Outline : 216-pin LQFP (24mm x 24mm x 1.4mm)





● Dimension (216-pin LQFP)

Dimension	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D	26.0 BSC		
D1	24.0 BSC		
E	26.0 BSC		
E1	24.0 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Y	0.08		
$\theta$	0°	3.5°	7°

Unit: mm

REF: Reference

BSC: Basic Spacing between Centers (integrated circuit package dimension)

9. Ordering Information

Part Number	Package	Status	Note
JL4229A	216-pin LQFP	Available	N/C



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