

JL4003B

High Speed USB 2.0 to ATA/ATAPI Bridge

The logo for JEILIN Technology Co., Ltd. is a large, stylized blue graphic. It features a large 'E' on the left, a vertical bar on the right, and a horizontal bar that connects them, with a circular element at the top right. The text 'Revision: 1.0' is centered over the logo.

Revision: 1.0

Date: **07/01/2005**

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0. Revision History

Revision	Description of Changes	Date
1.0	First Release	2005/07/01



1. General Description

JL4003B is a high performance and low cost USB 2.0 to ATA / ATAPI bridge controller. Integrated with high speed UTMI transceiver, its core includes both USB and ATA/ATAPI controllers and, additionally, a main processor unit to coordinate the data transmission between two controllers. As to one-chip design, JL4003B can support various kinds of ATA / ATAPI devices and fit in any compact, portable product design. To add the portability to the mass storage class peripherals for PC with USB 2.0 such as hard disk, CD-ROM, CD-R/RW, DVD-ROM and DVD±R/±RW. JL4003B is the best price/performance ratio choice of single-chip controller design.

2. Features

- Complies with ATA / ATAPI-6 Specification Rev 2.0(PIO mode 0~4, Multiple word DMA mode 0~2, and Ultra DMA mode 0~5)
- Complies with Universal Serial Bus Specification Rev. 2.0 (USB 2.0)
- Compliant to USB Mass Storage Class Specification, Version 1.0 (Bulk-Only Transport).
- Operating system supported: Window XP/2000/Me/98; Mac 9.X /10.X.
- Support 3 endpoints: (1) Control Pipe (2) Bulk Read (3) Bulk Write.
- Embedded a high-speed (UTMI) USB2.0 transceiver.
- Embedded a turbo microprocessor.
- External Program Memory: 16KB flash ROM supported. (Only for 100 pins package)
- 5V tolerance pad for IDE Interface.
- Apply to ATA/ATAPI Devices, such as Hard Disk, CD-ROM, CD-R/RW, DVD-ROM and DVD±R/±RW.
- Available in 48/64/100 pin LQFP package

3. Application

- USB2.0 Portable Storage Device
- External CD-RW (Combo Device)
- External DVD-RW
- External DVD±R/±RW



4. Block Diagram

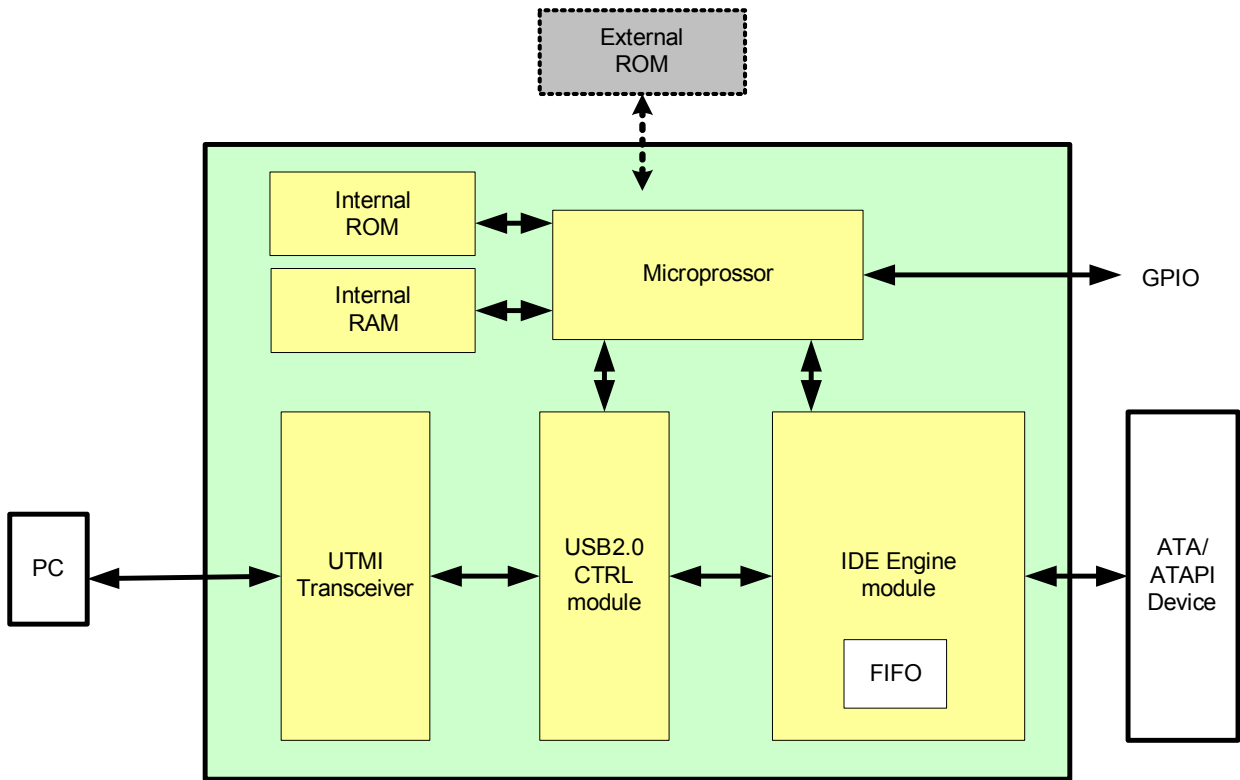


Figure 1: Block diagram



5. Pin Descriptions

● Pin Diagram

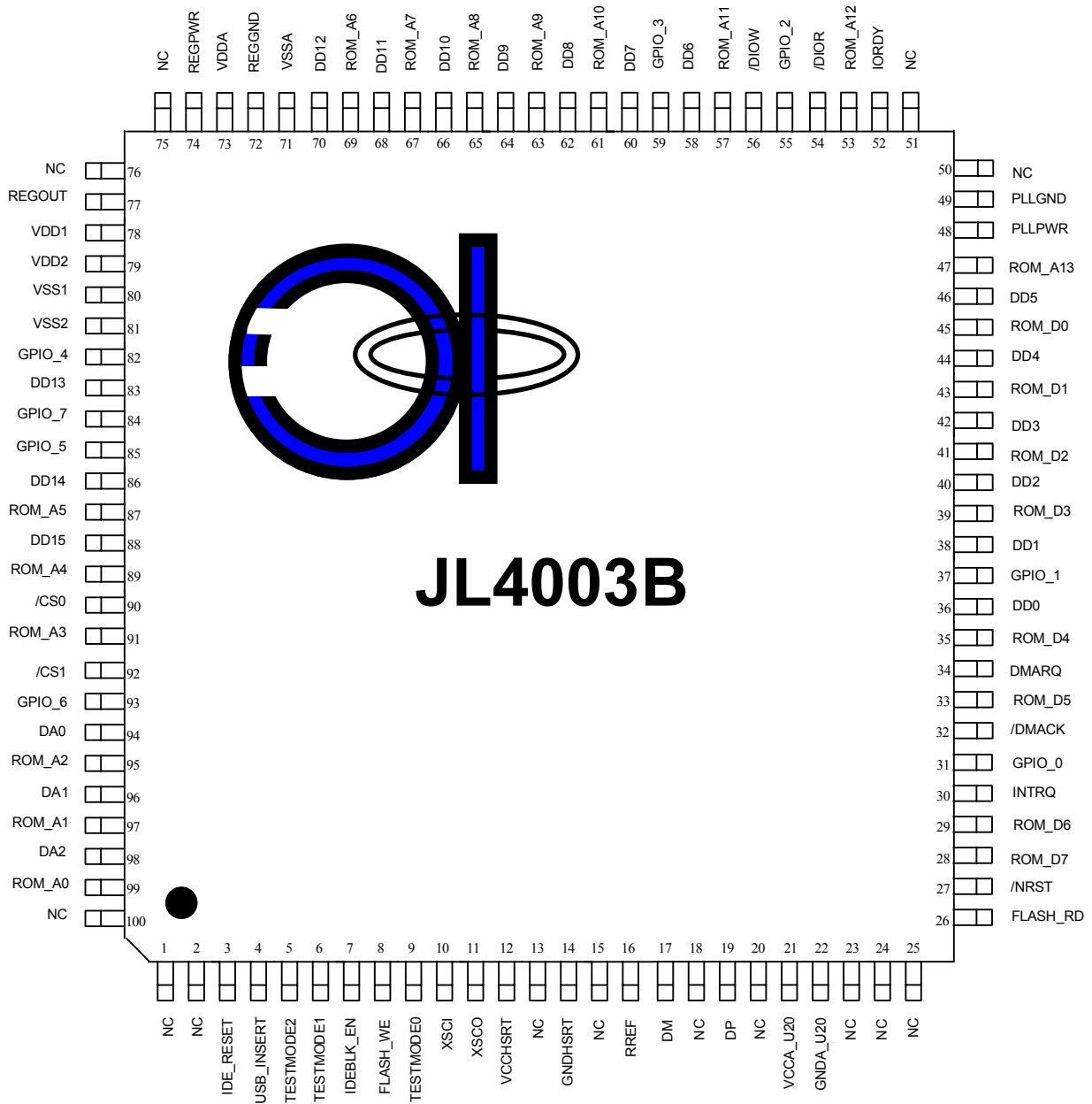


Figure 2: 100 Pin LQFP Pinout Diagram

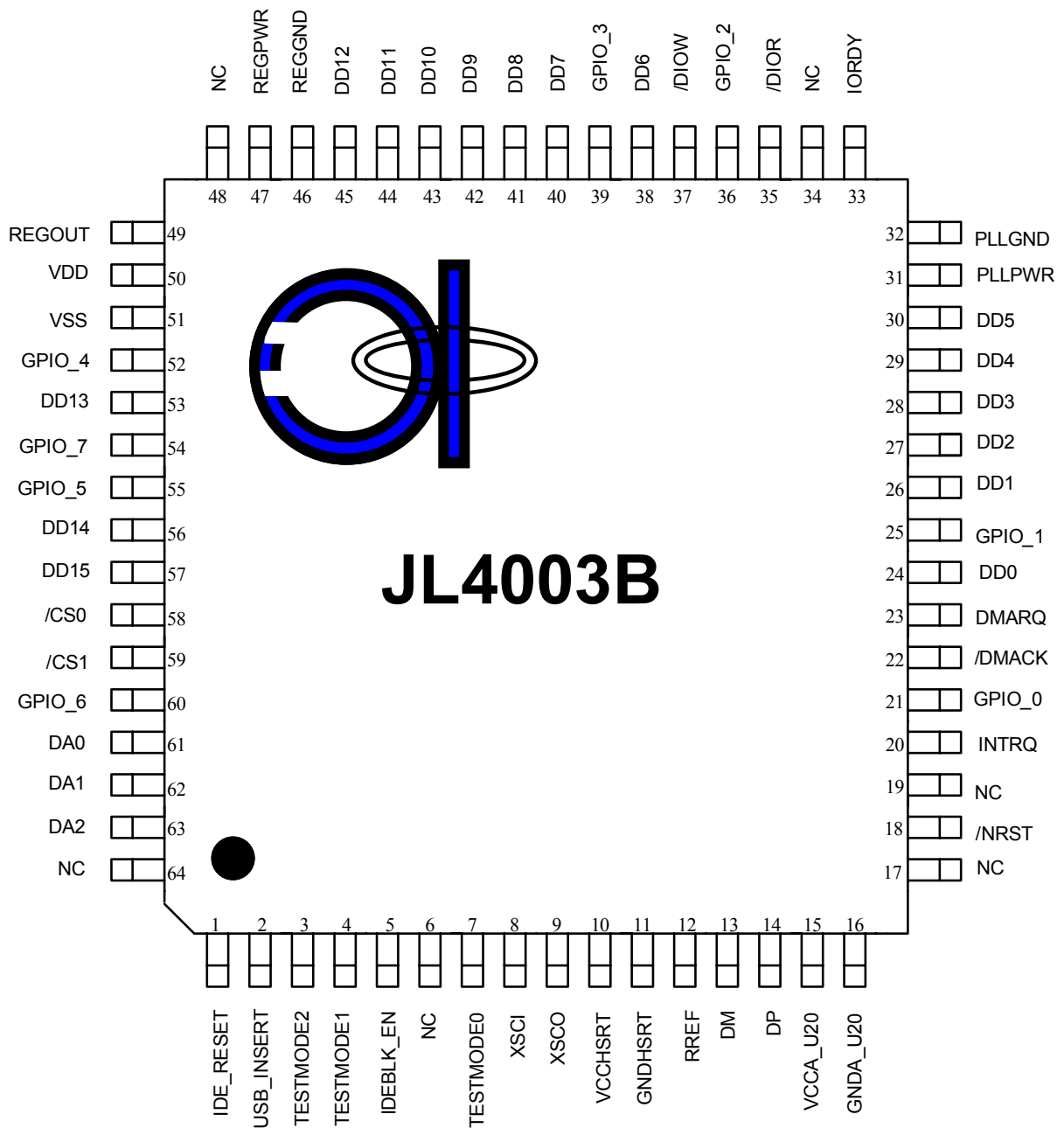


Figure 3: 64 pin LQFP Pinout Diagram

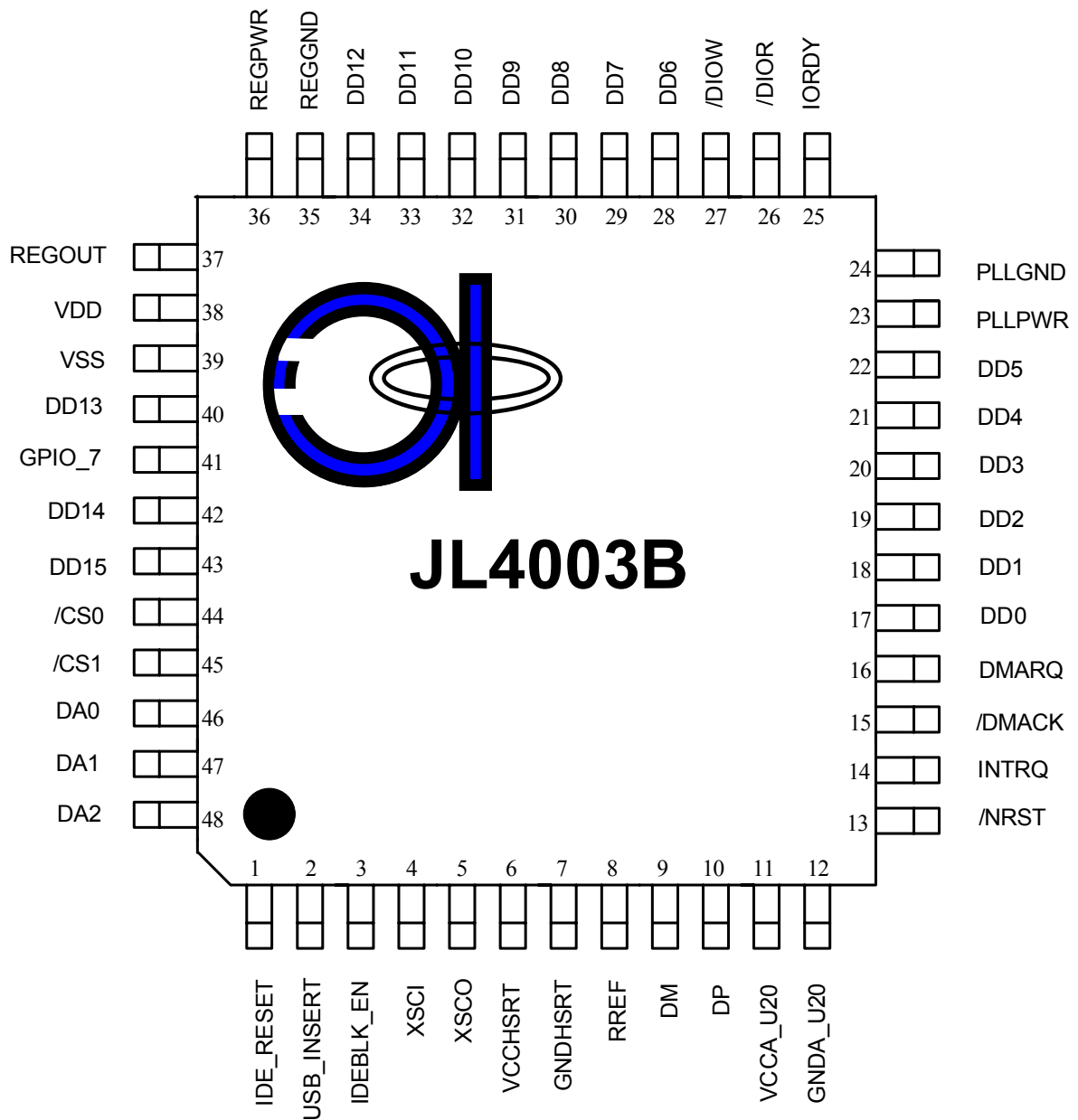


Figure 4: 48 pin LQFP Pinout Diagram



● Pin Descriptions

Pin Name	48 pin No.	64 pin No.	100 pin No.	Type	Description
IDE_RESET	1	1	3	B4	IDE hardware reset.
USB_INSERT	2	2	4	I	USB Inserted.
TESTMODE[2:0]	-	3, 4, 7	5, 6, 9	I,D	System test pin
IDEBLK_EN	3	5	7	I	IDE Block Enable, active high.
FLASH_WE	-	-	8	B2	Write Strobe of External Flash ROM.
XSCI	4	8	10	ICLK	Crystal terminal.
XSCO	5	9	11	OCLK	Crystal terminal
VCCHSRT	6	10	12	PWR	Analog supply voltage(3.3V)
GNDHSRT	7	11	14	GND	Analog ground supply.
REFF	8	12	16	AI	Connect external reference register(12K ohm +/- 1%) to Analog GND.
DM	9	13	17	USB	USB 2.0 Data Line(+)
DP	10	14	19	USB	USB 2.0 Data Line(-)
VCCA_U20	11	15	21	PWR	Analog supply voltage(3.3V)
GND_A_U20	12	16	22	GND	Analog ground supply.
FLASH_RD	-	-	26	B2	Read Strobe of External Flash Rom.
/NRST	13	18	27	I,S,U	Power on reset.
INTRQ	14	20	30	I,D	The active high interrupt request to the host.
/DMACK	15	22	32	B4	DMA acknowledge.
DMARQ	16	23	34	I,D	DMA request.
IORDY	25	33	52	I,U	IORDY/DDMARDY-/DSTROBE
/DIOR	26	35	54	B4	DIOR-/HDMARDY-/HSTROBE
/DIOW	27	37	56	B4	DIOW-/STOP
/CS[1:0]	45, 44	59, 58	92, 90	B4	Chip Select.
DA[2:0]	48, 47, 46	63, 62, 61	98, 96, 94	B4	IDE Address Line
DD[15:0]	43,42,40,34, 33,32,31,30, 29,28,22,21, 20,19,18,17	57,56,53,45, 44,43,42,41, 40,38,30,29, 28,27,26,24	88, 86, 83, 70, 68, 66, 64, 62, 60, 58, 46, 44, 42, 40, 38, 36	B4	IDE Data Bus
ROM_D[7:0]	-	-	28, 29, 33, 35,	I,D	Flash ROM Data Bus



Pin Name	48 pin No.	64 pin No.	100 pin No.	Type	Description
			39, 41, 43, 45		
ROM_A[13:0]	-	-	47, 53, 57, 61, 63, 65, 67, 69, 87, 89, 91, 95, 97, 99	B2	Flash ROM Address Bus
GPIO7	41	54	84	B2	General Purpose I/O
GPIO[6:0]	-	60, 55, 52, 39, 36, 25,21	93, 85, 82, 59, 55, 37, 31	B2	General Purpose I/O
PLLWDR	23	31	48	PWR	Analog supply voltage(2.5V)
PLLGND	24	32	49	GND	Analog ground supply.
REGWDR	36	47	74	PWR	Analog supply voltage(3.3V)
REGGND	35	46	72	GND	Analog ground supply.
REGOUT	37	49	77	AO	+2.5V power output of Internal Regulator.
VDDA	-	-	73	PWR	Analog supply voltage(3.3V)
VSSA	-	-	71	GND	Analog ground supply.
VDD1	38	50	78	PWR	Digital supply voltage(2.5V)
VSS1	39	51	80	GND	Digital ground supply.
VDD2	-	-	79	PWR	Digital supply voltage(2.5V)
VSS2	-	-	81	GND	Digital ground supply.
NC	-	6, 17, 19, 34, 48, 64	1, 2, 13, 15, 18, 20, 23, 24, 25, 50, 51, 75, 76, 100		No connect

Buffer Type Descriptions

Type	Description
I	Input Pin
O2	Output Pin with 2 mA drive
O4	Output Pin with 4 mA drive
B2	Bi-directional Pin with 2 mA drive
B4	Bi-directional Pin with 4 mA drive
B8	Bi-directional Pin with 8 mA drive
U	Internal weak pull-up resistor
D	Internal weak pull-down resistor



S	Schmitt Trigger
AI	Analog Input
AO	Analog Output
USB	USB Interface
ICLK	XTAL Clock Input
OCLK	XTAL Clock Output
PWR	Power Pin
GND	Ground Pin



6. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply (3.3V)	-0.3 to 3.6	V
V_{CC1}	Power Supply (2.5V)	-0.3 to 2.75	V
V_{IN}	Input Voltage	-0.3 to $V_{CC}+0.3$	V
V_{OUT}	Output Voltage	-0.3 to $V_{CC}+0.3$	V
T_{STG}	Storage Temperature	-55 to 150	°C

Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply (3.3V)	3.0	3.3	3.6	V
V_{CC1}	Power Supply (2.5V)	2.25	2.5	2.75	V
T_{OPR}	Operating Temperature	0	25	70	°C

DC Electrical Characteristics for 3.3 volts operation

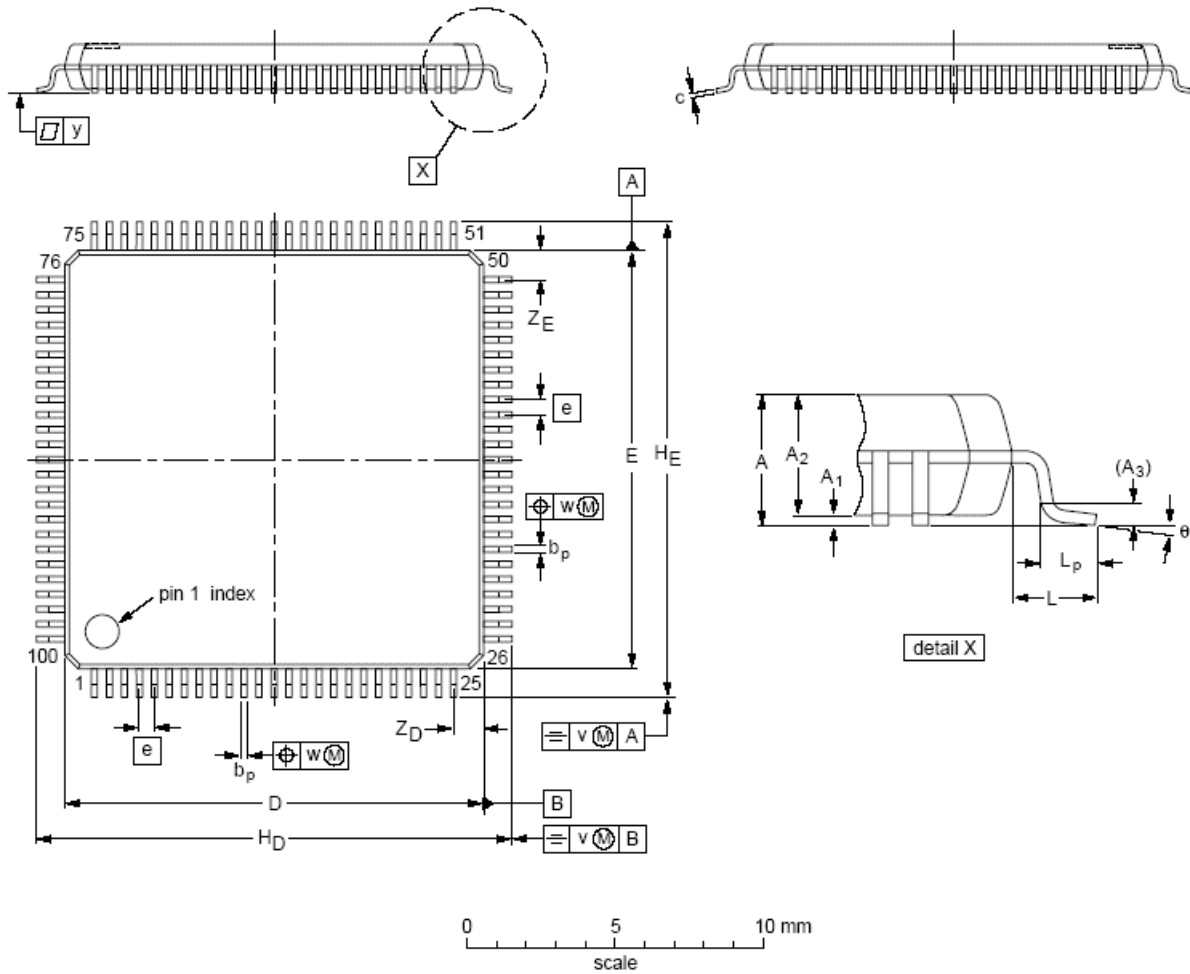
(Under Recommended Operating Conditions and $V_{CC} = 3.0V \sim 3.6V$, $T_j = 0^\circ C$ to $+70^\circ C$)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+0.3$	V
V_{T-}	Schmitt Input Low Voltage		-0.3		0.8	V
V_{T+}	Schmitt Input High Voltage		2.0		$V_{CC}+0.3$	V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V



7. Package Outline and Dimension

- Package Outline (100-pin LQFP)

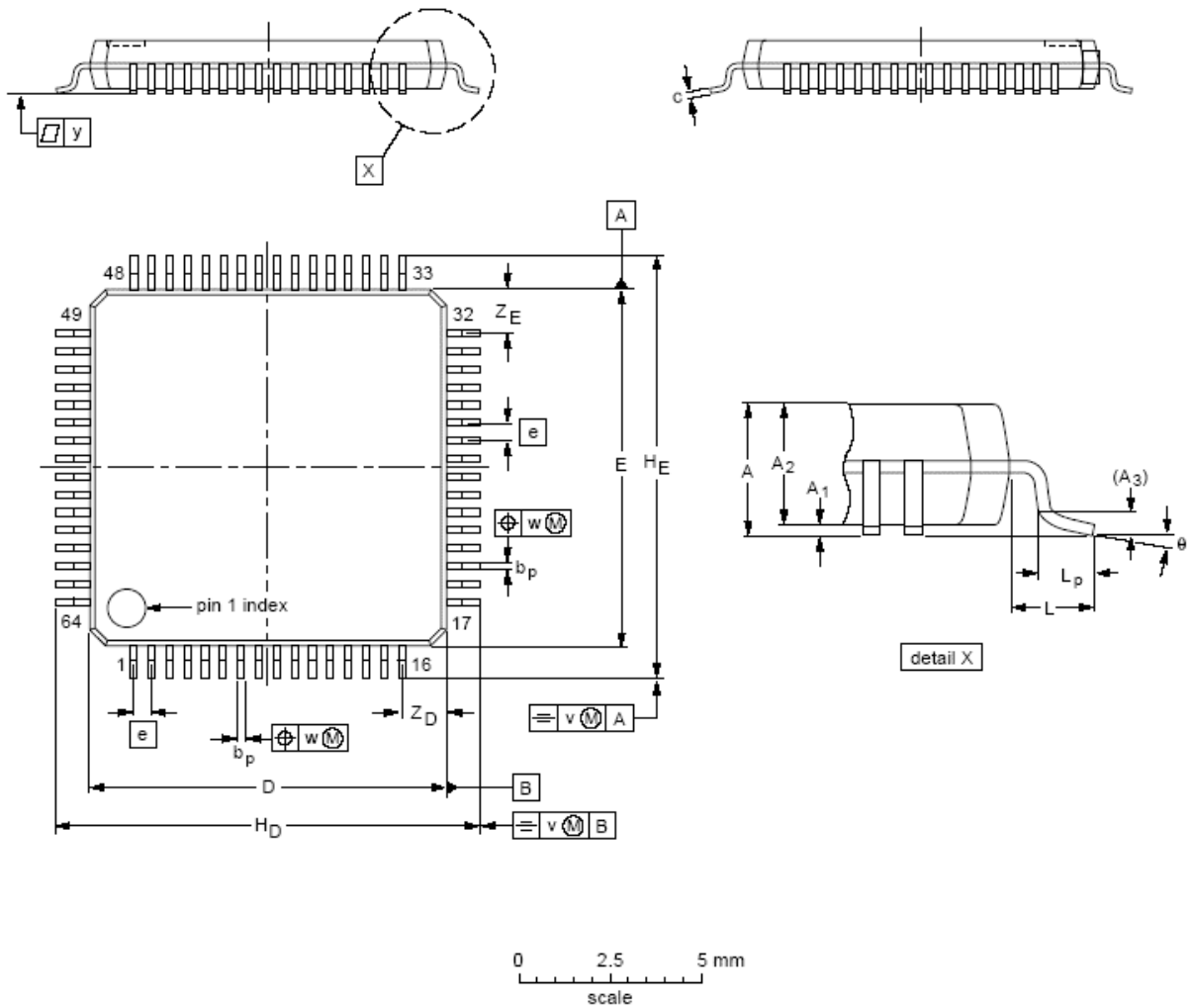


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°



● Package Outline (64-pin LQFP)

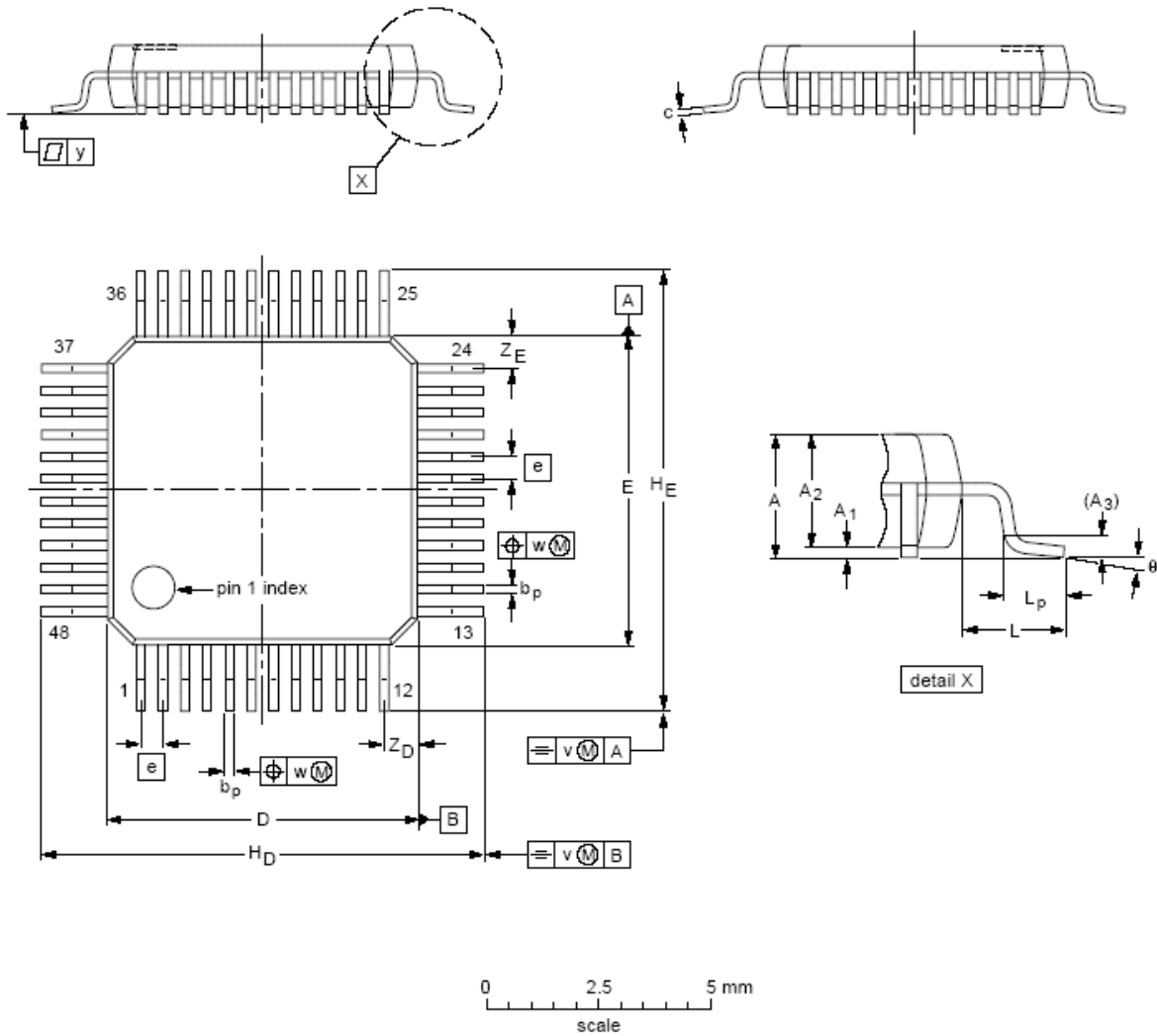


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°



● Package Outline (48-pin LQFP)



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°



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